Conclusion

Data show that it is presently feasible to construct low-noise GaAs FET amplifiers with performance comparable to uncooled parametric amplifiers. They exhibit the qualities of easy alignment, require little testing time, and demonstrate a high degree of gain stability. Saturation powers well in excess of those associated with parametric amplifiers are easily attained. The simplicity of the approach makes the cooled GaAs FET amplifier an attractive candidate as a second stage to a parametric amplifier. Using 1/2-μm GaAs FET's, it should be possible to realize noise temperatures well under 40 K in this frequency range.

The first-order analysis presented in this short paper for a simplified noise model of the FET yields results that correlate well with measurements.

Acknowledgment

The author wishes to thank L. Hernandez who did his usual outstanding job of assembling the unit.

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A Quasi-Linear Approach to the Design of Microwave Transistor Power Amplifiers

K. L. KOTZEBUE, MEMBER, IEEE

***Abstract*—A method of large-signal transistor characterization and power amplifier design is described which allows the designer to predict the load and source terminations required for optimum added-power circuit efficiency, and to see graphically how efficiency and power gain change as a function of the load termination. Experimental results obtained with a 1-W bipolar junction transistor (BJT) amplifier at 1.3 GHz are presented.**

Introduction

It is well known that microwave transistor power amplifiers are currently designed by largely empirical techniques [1], [2] since a suitable analytic approach has not been available. Perhaps one of the most successful large-signal design techniques to date has been the automatic load contour approach reported by Cusack *et al.* [3]. This technique is basically an automated version of the more conventional cut-and-try experimental approach to power amplifier optimization. Some limited success with a large-signal S-parameter characterization has also been reported [4]. In this short paper an analytic design approach is presented which is based upon a large-signal y-parameter characterization of high-frequency bipolar junction transistors (BJT's).

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The author is with the Department of Electrical Engineering and Computer Science, University of California, Santa Barbara, CA 93106.

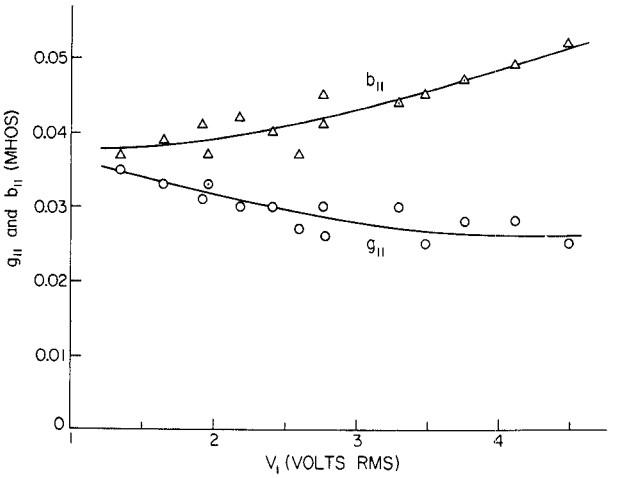

Fig. 1. Measured large-signal values of y_{11} for the CTC D1-28Z transistor at 1.3 GHz under fixed-bias conditions. V_{CC} = 20 V; I_C = 100 mA.

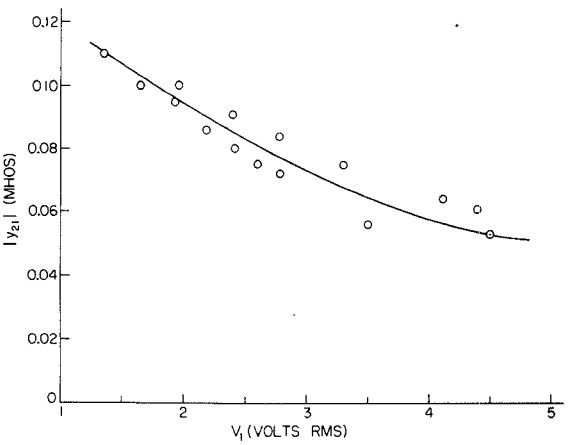

Fig. 2. Measured large-signal values of $|y_{21}|$ for the CTC D1-28Z transistor at 1.3 GHz under fixed-bias conditions. V_{CC} = 20 V; I_C = 100 mA. The angle of y_{21} remains constant at $-175°$.

Large-Signal Y-Parameter Characterization

In 1970, Houselander *et al.* [5] proposed that the large-signal behavior of a BJT in common-base or common-emitter configuration could be approximately characterized by a set of large-signal y parameters. In this characterization, y_{11} and y_{21} were considered to be functions of the input RF voltage V_1, while y_{12} and y_{22} were considered to be constant. The parameters y_{11} and y_{21} are most closely identified with the forward-biased base-emitter junction of the BJT, while the parameters y_{12} and y_{22} are most closely identified with the reverse-biased base-collector junction. Hence one would anticipate that most of the nonlinearity would be associated with the parameters y_{11} and y_{21}, provided that significant clipping does not occur at the output of the transistor. This assumption of no significant clipping at the output of the BJT appears to be valid in high-frequency operation. A good discussion of this approach to the large-signal characterization of a high-frequency BJT may be found in Spence [6].

For this investigation, measurements were made of the large-signal y parameters of a silicon BJT rated at 1-W output at 960 MHz (CTC D1-28Z) using a measurement technique described in [7]. Figs. 1–4 show the measured results for a typical device at 1.3 GHz when biased to V_{CC} = 20 V, I_C = 100 mA.

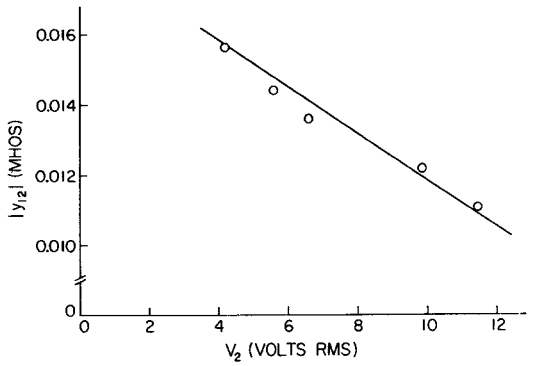

Fig. 3. Measured large-signal values of $|y_{12}|$ for the CTC D1-28Z transistor at 1.3 GHz under fixed-bias conditions. V_{CC} = 20 V; I_C = 100 mA. The angle of y_{12} remains constant at −134°.

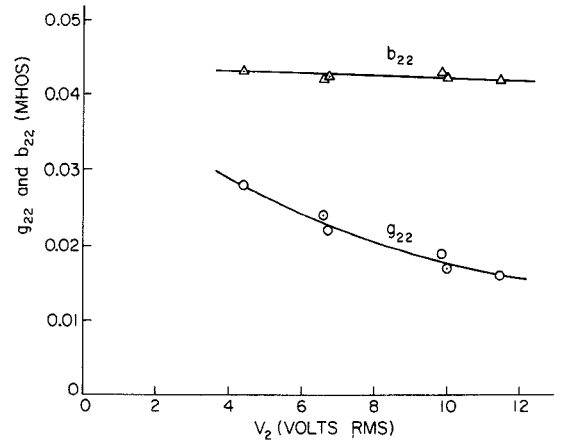

Fig. 4. Measured large-signal values of y_{22} for the CTC D1-28Z transistor at 1.3 GHz under fixed-bias conditions. V_{CC} = 20 V; I_C = 100 mA.

The data as presented in these figures seem somewhat in conflict with the proposal and data of Houselander *et al.* [5] that y_{12} and y_{22} can be considered independent of the RF amplitude. Our present feeling is that the proposed model of constant y_{12} and y_{22} is reasonable for the microwave BJT, but that series parasitic elements have made it impossible to completely short circuit the base-emitter junction. The amount of variation indicated has not caused difficulty, as will be demonstrated in the section on experimental results.

The Design Technique

A useful amplifier design technique which is primarily concerned with added-power circuit efficiency may be obtained by a modification of the well-known graphical technique originated by Linvill and Schimpf [8]. However, instead of determining contours of constant power gain, in the present approach contours of constant added power are obtained.

The added power P_a is defined as the difference between the output RF power and the input RF power:

$$P_a \equiv P_{\text{out}} - P_{\text{in}}. \tag{1}$$

A normalized added power p_a is defined as

$$p_a \equiv \frac{4P_a g_{22}}{|y_{21}|^2 |V_1|^2} \tag{2}$$

where V_1 is the amplitude of the RF voltage at the input of the transistor.

In the (x,y) coordinate system which is used in the conventional Linvill chart representation [6], [9], the following expression involving the normalized added power may be derived:

$$\left[x + \left|\frac{y_{12}}{y_{21}}\right|\right]^2 + y^2 = 1 + \left|\frac{y_{12}}{y_{21}}\right|^2 - \frac{2}{C}\left|\frac{y_{12}}{y_{21}}\right| - p_a \tag{3}$$

where

$$C \equiv \frac{|y_{21}y_{12}|}{2g_{11}g_{22} - \text{Re}\,(y_{21}y_{12})}.$$

Equation (3) thus defines a family of circles of constant added power. The centers of all circles are identical, located at

$$x_0 = -\left|\frac{y_{12}}{y_{21}}\right|, \qquad y_0 = 0 \tag{4}$$

with radii given by

$$r = \left[1 + \left|\frac{y_{12}}{y_{21}}\right|^2 - \frac{2}{C}\left|\frac{y_{12}}{y_{21}}\right| - p_a\right]^{1/2}. \tag{5}$$

The maximum value of added power will occur when the radius is equal to zero. The result, as obtained from (5), is

$$(P_a)_{\max} = |V_1|^2 \frac{|y_{21}|^2 + |y_{12}|^2 + 2\,\text{Re}\,(y_{21}y_{12}) - 4g_{11}g_{22}}{4g_{22}}. \tag{6}$$

The load termination corresponding to the point of maximum added power is given by

$$(Y_L)_{\text{opt}} = \frac{2y_{21}g_{22}}{y_{21} + y_{12}^*} - y_{22}. \tag{7}$$

For the case of $y_{21} \gg y_{12}$, this becomes

$$(Y_L)_{\text{opt}} \simeq y_{22}^*. \tag{8}$$

The input admittance with the optimum load termination is given by

$$(Y_{\text{in}})_{\text{opt}} = y_{11} - \frac{y_{21}y_{12} + |y_{12}|^2}{2g_{22}}. \tag{9}$$

With V_1 held constant, different positions on the Linvill chart imply different values of V_2; hence if y_{12} and y_{22} are functions of V_2 this design procedure cannot be exact. In practice, however, we are primarily interested in amplifier behavior over a narrow range of V_2 near saturation; therefore, useful information can be obtained even if y_{12} and y_{22} vary with the RF amplitude V_2. The physical interpretation of a circle defined by (4) and (5) is that it represents a contour of constant added power for a given value of input voltage V_1. Under conditions of amplifier saturation, such a circle will also represent a useful contour of constant added-power circuit efficiency.

Experimental Results

Since the measured data show y_{12} and y_{22} at 1.3 GHz to be functions of the RF voltage V_2, some ambiguity exists as to which values are the most appropriate to use as a starting point in the design. Experimental results indicate that the most appropriate values of y_{12} and y_{22} are those which are measured at peak values of V_2 which are comparable to V_{CC}. An appropriate value of V_1 can be determined by calculating the added power as given by (6), and selecting the value of V_1 which maximizes the added power. In the present case, $V_1 \simeq 4.5$ V was selected as most appropriate, which results in a predicted value of 660 mW for

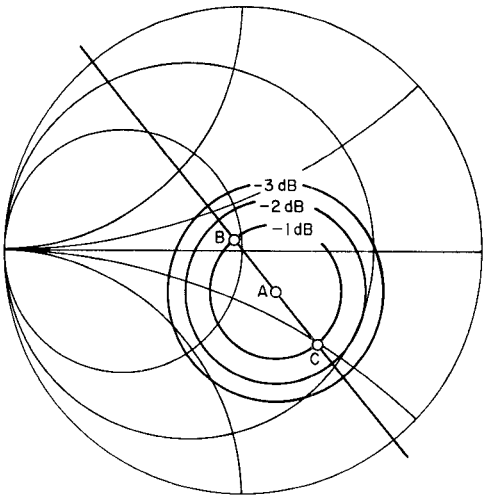

Fig. 5. The added-power Linvill chart for the 1.3-GHz transistor, showing three contours of constant added power and three designs which were experimentally investigated.

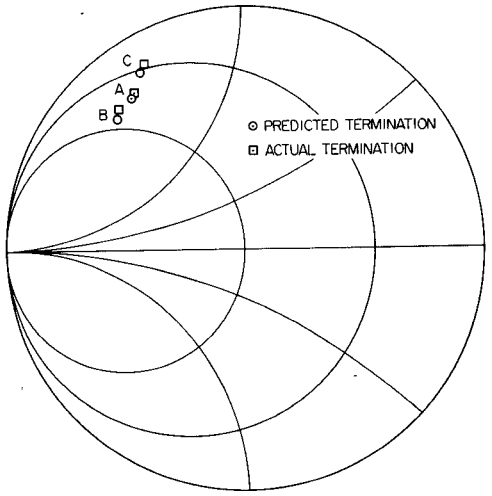

Fig. 6. A Smith chart admittance representation showing the comparison between the predicted and actual load terminations for the three designs of Fig. 5.

the added power. The values of the resulting large-signal y parameters are given as follows:

$$y_{11} = 0.025 - j0.052 \text{ mho}$$

$$y_{12} = -0.0076 - j0.008 \text{ mho}$$

$$y_{21} = -0.053 - j0.005 \text{ mho}$$

$$y_{22} = 0.016 + j0.042 \text{ mho}.$$

The added-power Linvill chart representation for this set of y parameters is shown in Fig. 5, with three contours of constant added power shown. These three contours represent values of added power which are 1, 2, and 3 dB below the maximum value, with the maximum added power occurring at the center of the circles. The points labeled A, B, and C represent three different load terminations which were experimentally investigated. Each load termination was preset and then experimentally adjusted as required. The load termination for design A was optimized for maximum added power, while the load terminations for designs B and C were adjusted to yield saturated added power approximately 1 dB below that which was measured for design A.

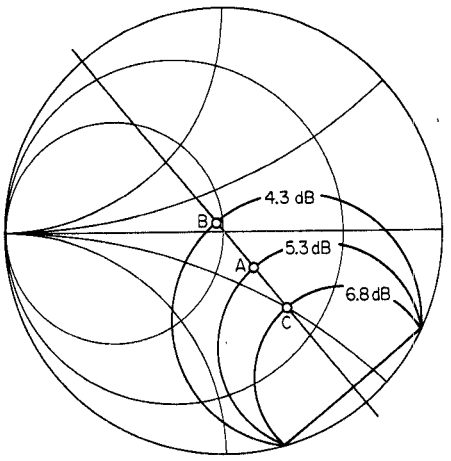

Fig. 7. A conventional Linvill chart for the 1.3-GHz transistor showing the contours of constant power gain which are applicable to the three designs of Fig. 5.

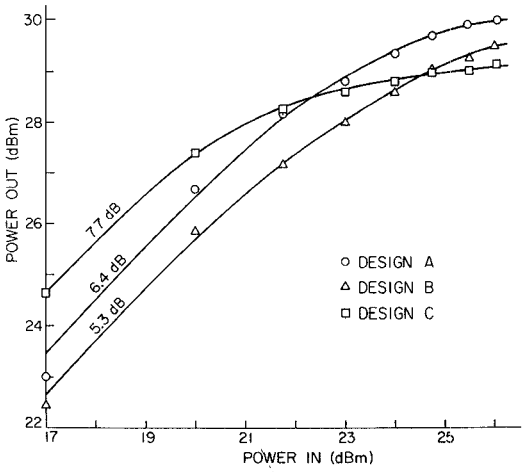

Fig. 8. Experimentally measured output power as a function of input power for the three designs of Fig. 5.

Fig. 6 shows a comparison between the predicted load terminations and the experimentally measured terminations for each design. The agreement is considered to be good. The maximum measured added power for this transistor was 630 mW, yielding an added-power circuit efficiency of 31.5 percent and a collector efficiency of 50 percent. The measured large-signal input admittance of the design A amplifier was 0.008 mho − j0.058 mho, while the value predicted from (9) was 0.010 mho − j0.066 mho.

Another important aspect of this design approach is that it is possible to show contours of constant power gain as well as contours of constant added power; hence the designer can see at a glance how power gain and circuit efficiency are interrelated. The contours of constant power gain are obtained from a conventional Linvill analysis; Fig. 7 shows such a Linvill chart representation. From the graphical construction we determine that design A should have a power gain of 5.3 dB, design B a power gain of 4.3 dB, and design C a power gain of 6.8 dB. These gains should be achieved at the value of V_1 appropriate to the large-signal y parameters used in the construction of the Linvill chart, which was chosen to approximately maximize the added power. Fig. 8 shows the experimentally measured power gain characteristic of each of the three designs. It is of interest to note that in each case the predicted large-signal power gain

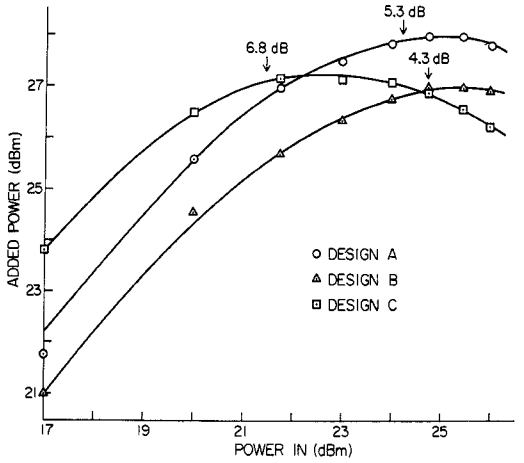

Fig. 9. Experimentally measured added power as a function of input power for the three designs of Fig. 5.

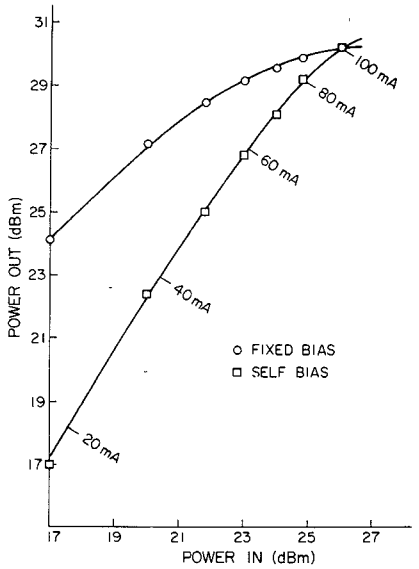

Fig. 10. Experimentally measured output power as a function of input power for the amplifier of design A, under both fixed-bias operation and self-bias operation. For fixed-bias operation, V_{CC} = 20 V; I_C = 100 mA. For self-bias operation, V_{CC} = 20 V, and I_C is as indicated in the figure.

is approximately 1 dB less than the measured small-signal power gain. The data of Fig. 8 are replotted in Fig. 9 to show that the predicted values of large-signal power gain did indeed occur near the point of maximum added power.

All of the preceding data are for fixed-bias operation (class A operation). In many cases, however, a microwave transistor power amplifier is operated under self-bias conditions (class C operation). The question arises whether the design procedure described here also applies to such self-bias operation. To investigate, the test amplifier was modified for self-bias operation by grounding the base bias lead. The results of this test are shown in Fig. 10. This figure shows that the performance of the self-biased amplifier became identical to the performance of the fixed-bias amplifier at the exact point where the self-bias operating point became identical to the fixed-bias operating point. Hence this design approach appears to be valid for both fixed-bias and self-bias amplifiers.

Conclusion

A method of large-signal device characterization and power amplifier design has been described and shown to be valid for a 1-W silicon BJT operating at 1.3 GHz. This approach not only allows the designer to predict the load and source terminations required for optimum added-power circuit efficiency, but also graphically shows how efficiency and power gain change with different load terminations. The method is felt to be generally applicable at frequencies sufficiently high such that significan clipping does not occur at the output of the device. While the precise lower limit of this frequency range is not presently known, experimental results indicate that it should be valid for those frequencies where the added-power circuit efficiency is 50 percent or less.

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Passive Millimeter-Wave IC Components Made of Inverted Strip Dielectric Waveguides

R. RUDOKAS AND T. ITOH, SENIOR MEMBER, IEEE

***Abstract*—New directional couplers and ring resonators for millimeter-wave IC's were fabricated from the inverted strip (IS) dielectric waveguide. They were tested in the 75–80-GHz range, and the agreement between the theoretical and experimental results was found to be good.**

I. Introduction

Inherent limitations in conventional metal waveguides at millimeter wavelengths have spurred research into alternate guiding structures [1]–[4]. In particular, the inverted strip (IS) dielectric waveguide [5] shows promise from the standpoint of low loss, ease of fabrication, and convenient size. Comparison

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R. Rudokas is with the Coordinated Science Laboratory and the Department of Electrical Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801.

T. Itoh was with the Coordinated Science Laboratory and the Department of Electrical Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801. He is now with the Stanford Research Institute, Menlo Park, CA 94025.